



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,437	03/24/2004	Ho-Woo Park	SEC.1135	4263

20987 7590 09/06/2005

VOLENTINE FRANCO, & WHITT PLLC
ONE FREEDOM SQUARE
11951 FREEDOM DRIVE SUITE 1260
RESTON, VA 20190

EXAMINER

THOMAS, TONIAE M

ART UNIT	PAPER NUMBER
----------	--------------

2822

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary

Application No.

10/807,437

Applicant(s)

PARK ET AL.

Examiner

Toniae M. Thomas

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 6-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>03/24/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This is a first Office action on the merits of Application Serial No. 10/807,437. Currently, claims 1-20 are pending.

Election/Restrictions

2. Applicant's election without traverse of Group I, claims 1-5, in the reply filed on 19 August 2005 is acknowledged. Claims 6-20 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

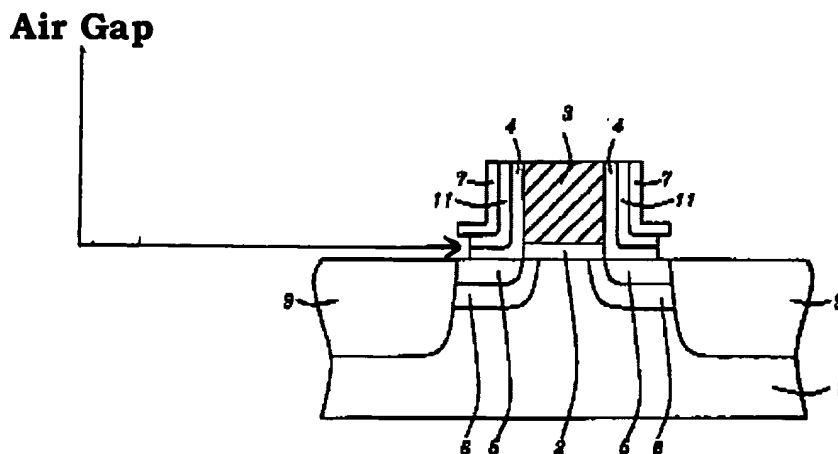
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Quek (US 6,924,180 B2).

Quek discloses a semiconductor device (see figs. 1-6 and accompanying text). The device comprises: a semiconductor substrate 1 having source/drain regions 9 spaced from each other (see fig. 5 and col. 4, lines 14-17); a gate

Art Unit: 2822

pattern 3 disposed on the semiconductor substrate between the source/drain regions (see fig. 5 and col. 3, lines 15-18); L-shaped spacers 7 each including a vertical portion covering a respective one of the side walls of the gate pattern, and a lateral portion extending laterally from the bottom of the vertical portion over a respective one of the source/drain regions (see fig. 5 and col. 4, lines 4-14); and support portions 11 interposed between the L-shaped spacers 7 and the gate pattern 3 (see fig. 5 and col. 3, lines 58-63), the support portions supporting the L-shaped spacers such that the lateral portion of each of the L-shaped spacers is spaced above the source/drain regions 9 over which the lateral portion of the L-shaped spacer extends, and wherein an air gap exists between the lateral portion of each of the L-shaped spacers and the source/drain region over which the lateral portion extends (see fig. 5 and col. 4, lines 42-49).

**FIG. 5**

The source/drain region 9 comprises a lightly doped source/drain region 5 over which the lateral portion of one of the L-shaped spacers extends (see fig. 5 and col. 3, lines 40-44), and a highly doped source/drain region 9 disposed laterally of the lateral portion of the L-shaped spacer 7 (see fig. 5 and col. 4, lines 14-17).

A buffer insulating layer 4 is interposed between the gate pattern and the support portion (see fig. 5 and col. col. 3, lines 26-29).

Claim Rejections - 35 USC § 103

4. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quek.

Quek does not teach that the L-shaped spacers 7 comprise an oxide layer, as recited in claim 3, or that the support portions 11 comprise a polysilicon layer or a nitride layer, as recited in claim 4. On the contrary the L-shaped spacers comprise a nitride layer (col. 4, lines 4-14), and the support portions comprise an oxide layer (col. 3, lines 58-63).

An etching process is used to form the structure shown in fig. 5. To form this structure, it is essential that the materials used for the spacers 8, the L-shaped spacers 7, and the support portions 11 are chosen so that adjacent layers have different etching rates with respect to one another. For example, the material used for the spacers 8 is silicon oxide, while the material used for the L-shaped spacers 7, which are adjacent to the spacers 8, is silicon nitride. Likewise, silicon oxide is the material used for the support portions 11, which

Art Unit: 2822


are adjacent to the L-shaped spacers 7. Alternating layers of silicon nitride and silicon oxide are used for the spacers 8, the L-shaped spacers 7, and the support portions 11 because silicon oxide and silicon nitride have different etching rates with respect to one another. Since silicon oxide and silicon nitride have different etching rates with respect to one another, using a nitride layer for the oxide spacers 8, an oxide layer for the L-shaped spacers 7, and a nitride layer for the support portions 11 is an obvious modification of Quek. In addition, because polysilicon and silicon oxide have different etching rates with respect to one another, it would have been obvious to the skilled artisan, at the time the invention was made, to use polysilicon in place of silicon nitride.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
26 August 2005



AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800